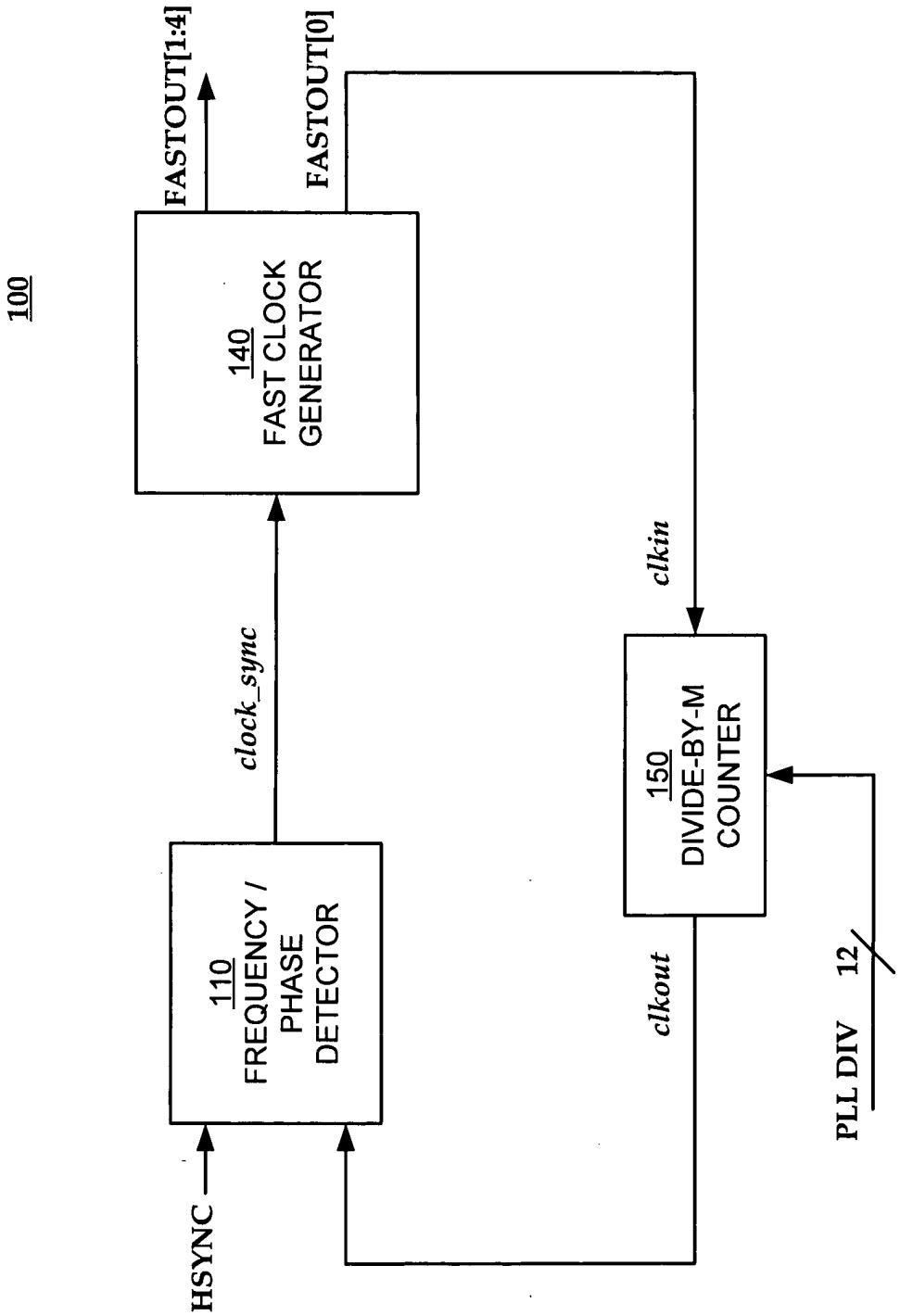

100
FASTOUT[1:4]
FASTOUT[0]
140
FAST CLOCK GENERATOR
clkin
clock_sync
150
DIVIDE-BY-M COUNTER
110
FREQUENCY / PHASE DETECTOR
clkout
PLL DIV
12
HSYNC

FIGURE 1

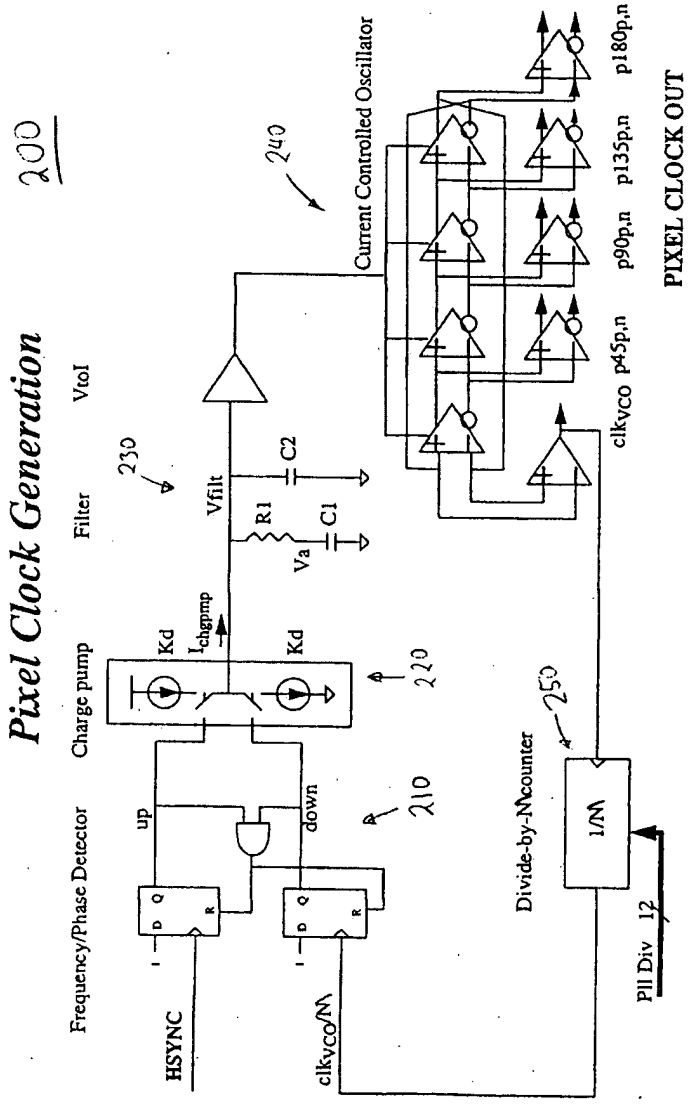

Pixel Clock Generation
200
Frequency/Phase Detector
Charge pump
Filter
VtoI
Current Controlled Oscillator
240
230
220
210
250
Vfilt
C2
R1
C1
Va
Kd
Kd
Ichgpmp
up
down
HSYNC
clkVCO/N
Divide-by-Ncounter
1/N
Pll Div 12
clkVCO p45p,n
p90p,n
p135p,n
p180p,n
PIXEL CLOCK OUT

FIGURE 2

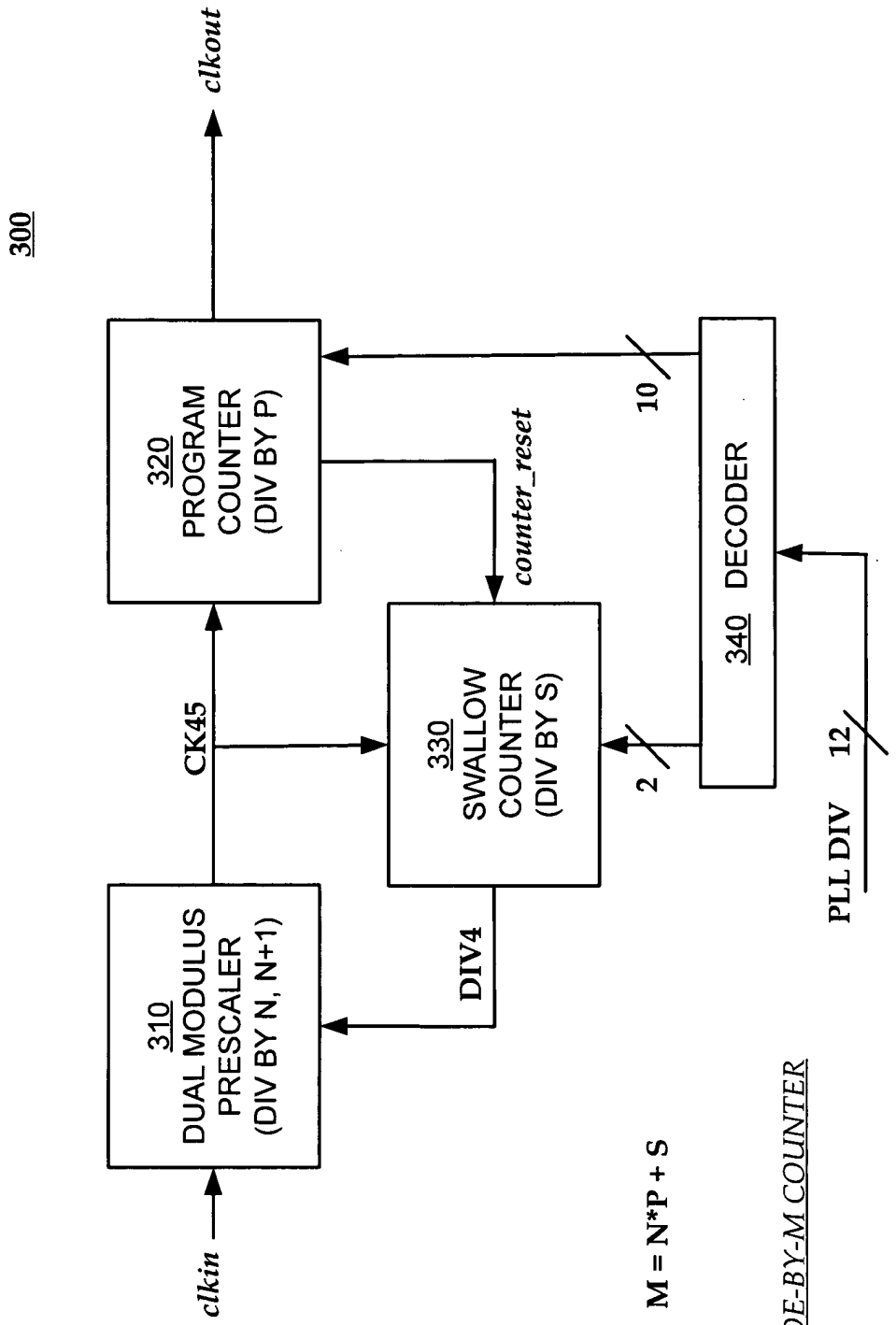

300
clkout
320 PROGRAM COUNTER (DIV BY P)
10
counter_reset
340 DECODER
CK45
330 SWALLOW COUNTER (DIV BY S)
2
12
PLL DIV
310 DUAL MODULUS PRESCALER (DIV BY N, N+1)
DIV4
clkin
M = N*P + S
DIVIDE-BY-M COUNTER

FIGURE 3

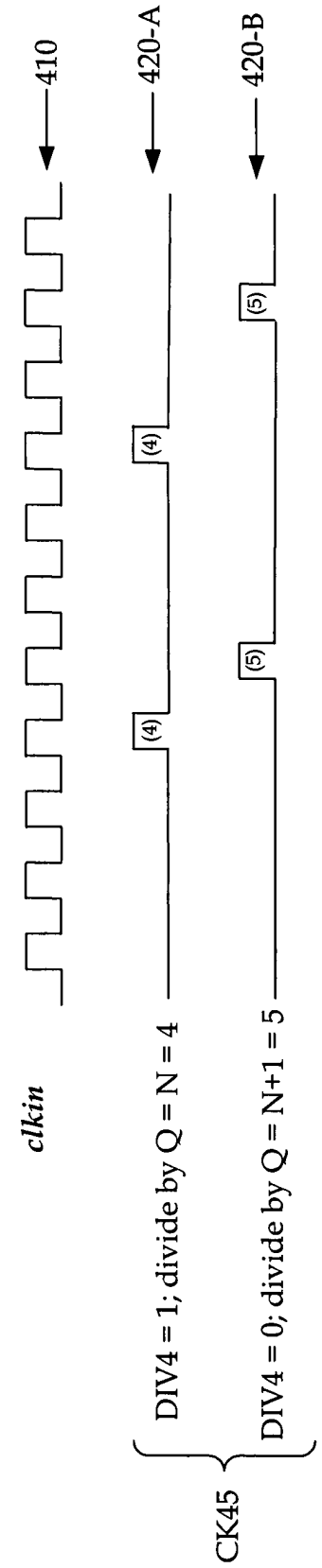


FIGURE 4A

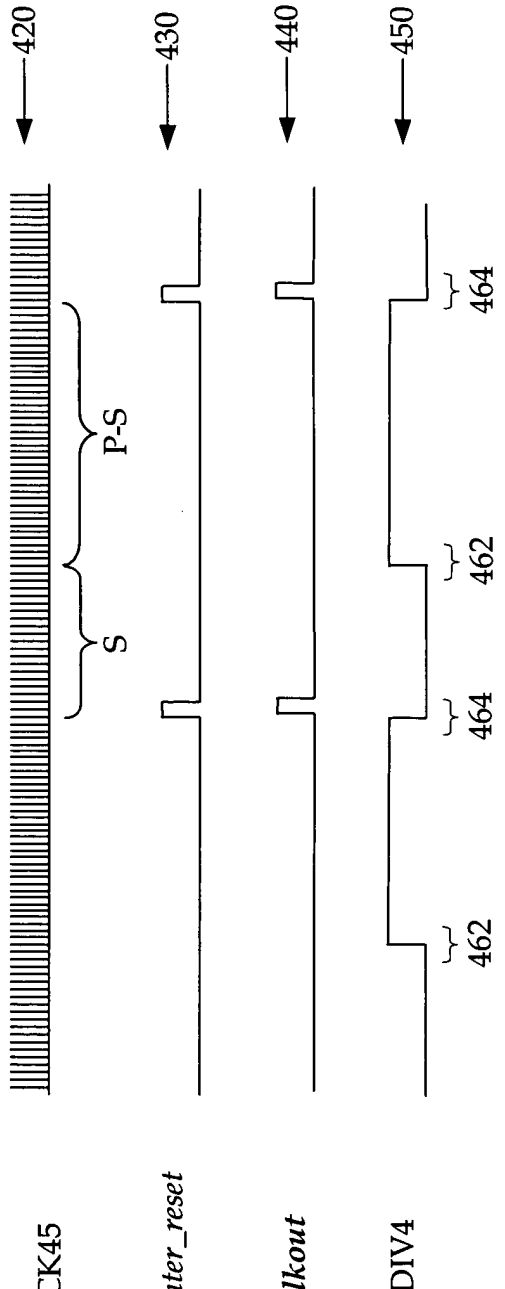


FIGURE 4B

500

M	DIV ← M-1	P← DIV[11:2]	S← DIV[1:0]
(12 bit)	(12bit)	(10 bit)	(2 bit)
(values)		(values)	(values)
17-20	...	4	0-3
21-24		5	0-3
25-28		6	0-3
29-32		7	0-3
33-36		8	0-3
37-40		9	0-3
...		...	
1009-1013		252	0-3
...		...	
2033-2036		508	0-3
...		...	
3073-3076		768	0-3
...		...	
4093-4096		1023	0-3

M = N*P + S

FOR N=4

FIGURE 5

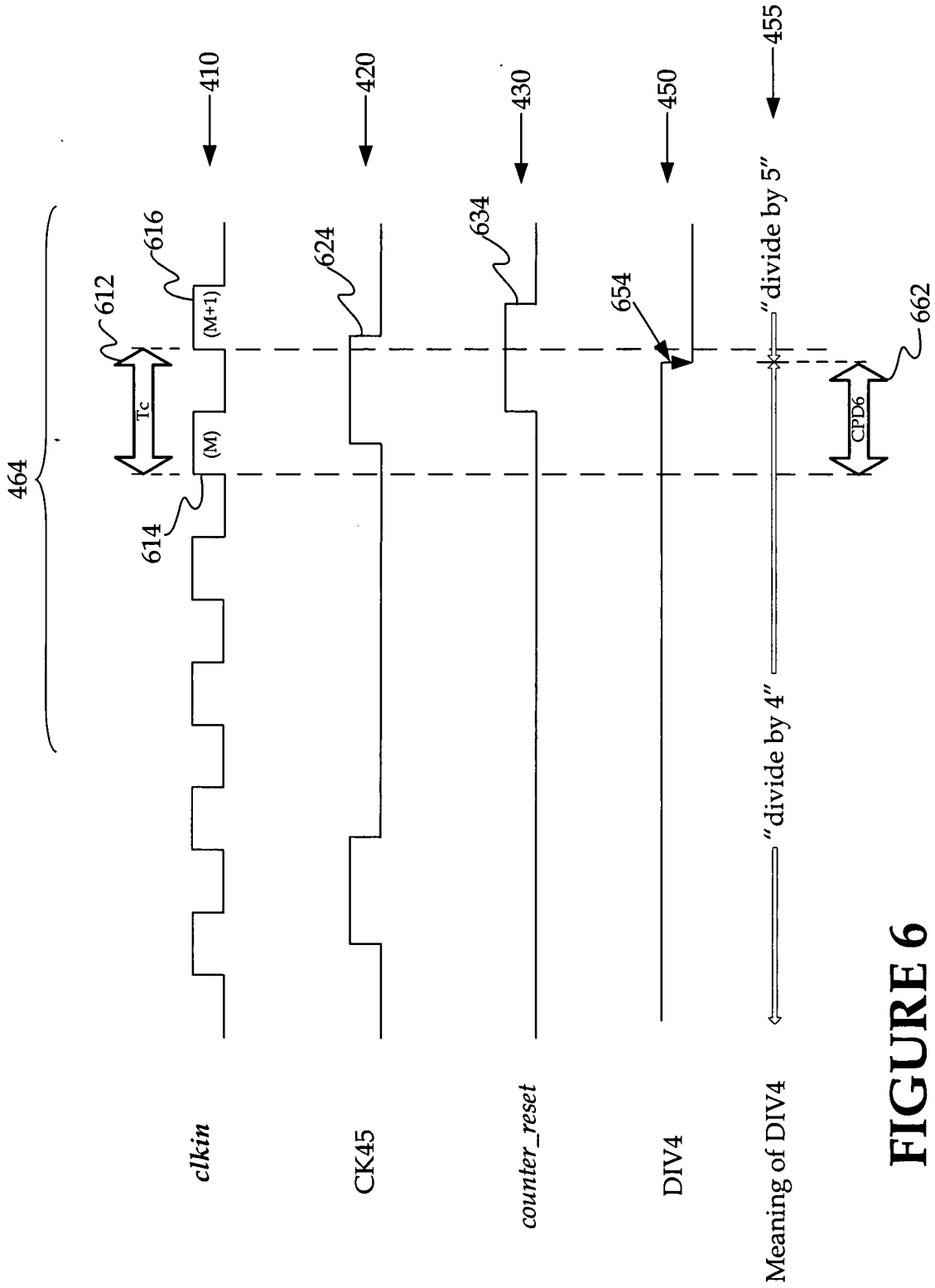

464
410
420
430
450
455
612
616
624
634
654
662
(M+1)
(M)
Tc
614
CPD6
"divide by 5"
"divide by 4"
clkin
CK45
counter_reset
DIV4
Meaning of DIV4

FIGURE 6

N = 4

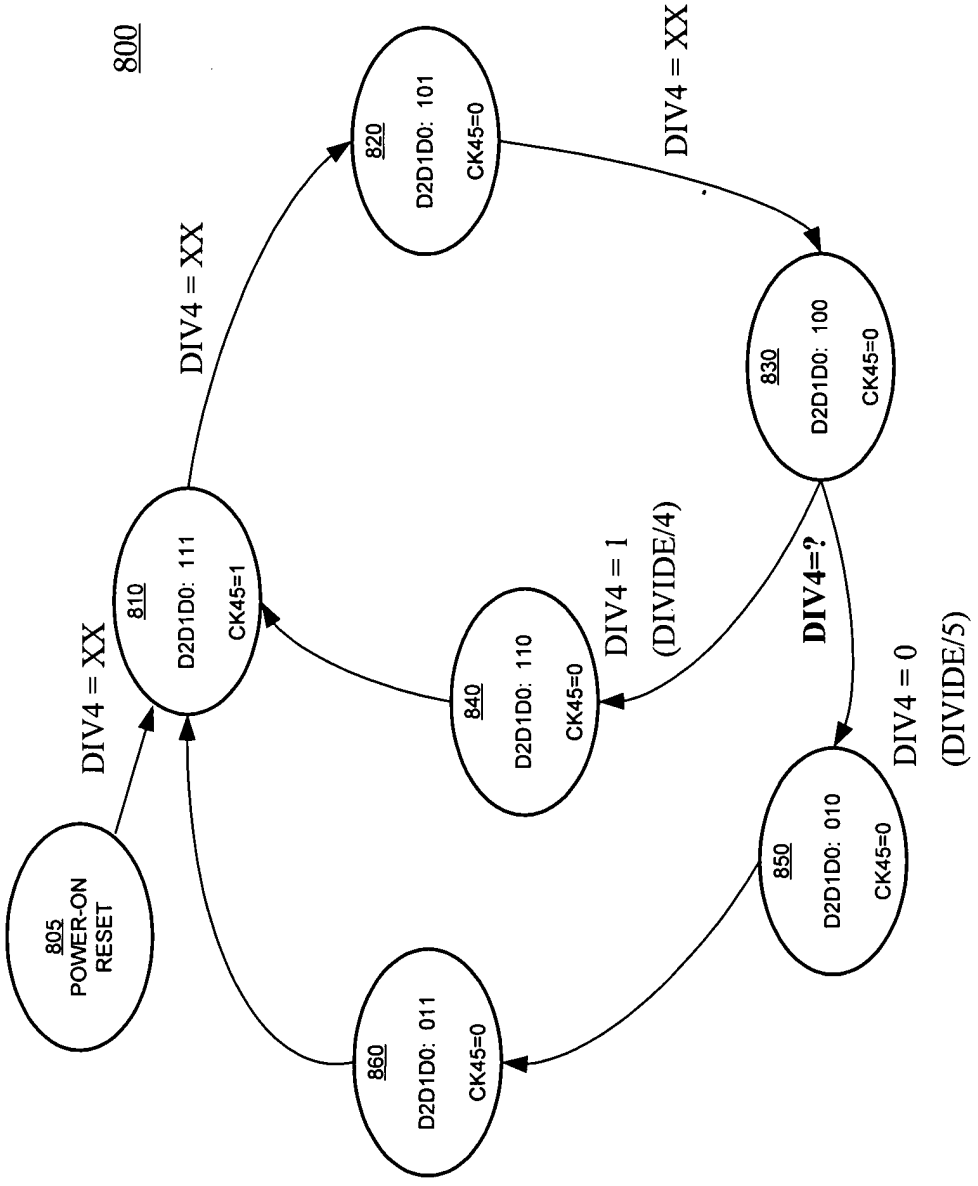
VARIABLE TYPE	SYMBOL	START (AT POR)	NEXT ASSIGNED VALUE
INTERNAL	D2	1	NEXT_D2 = DIV4 OR D0
INTERNAL	D1	1	NEXT_D1 = ~(D2 AND D0)
INTERNAL	D0	1	NEXT_D0 = D1
OUTPUT	CK45	1	NEXT_CL45 = D2 AND D1 AND D0

PRESCALER LOGIC

XX = DON'T CARE

FIGURE 7

DRAWING FOR PATENT APPLICATION
DARBY & DARBY P.C., USPTO CUSTOMER NO. 38845
ATTORNEY DOCKET NO: 08211-0200374-US0
INVENTOR: Ha Chu Vu
TITLE: PRESCALING FOR DIVIDING FAST PULSED SIGNAL



PRESCALER STATE MACHINE

FIGURE 8

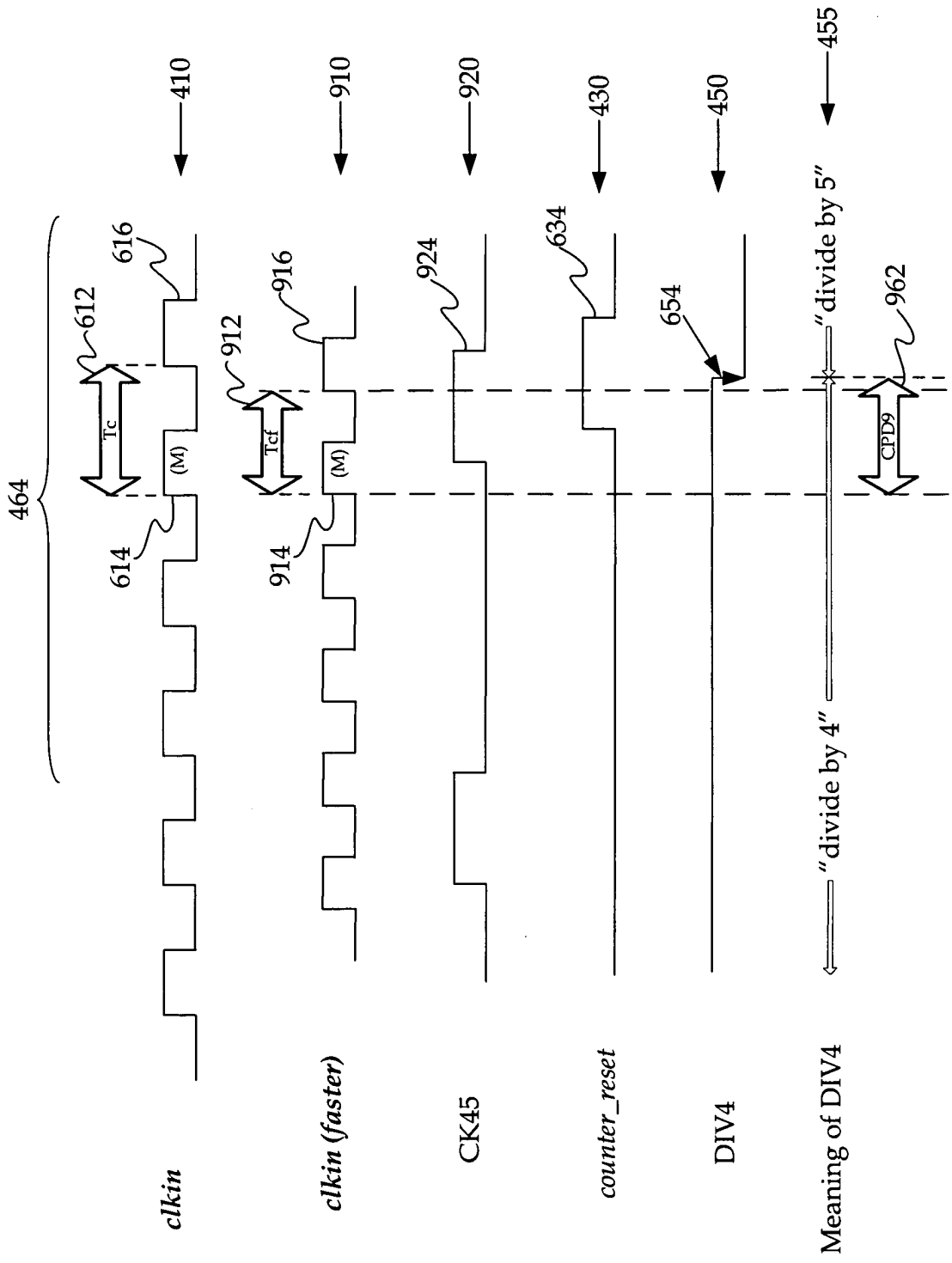

464
410
910
920
430
450
455
612
616
912
916
924
634
654
962
614
914
Tc
Tcf
(M)
(M)
CPD9
"divide by 5"
"divide by 4"
clkin
clkin (faster)
CK45
counter_reset
DIV4
Meaning of DIV4

FIGURE 9

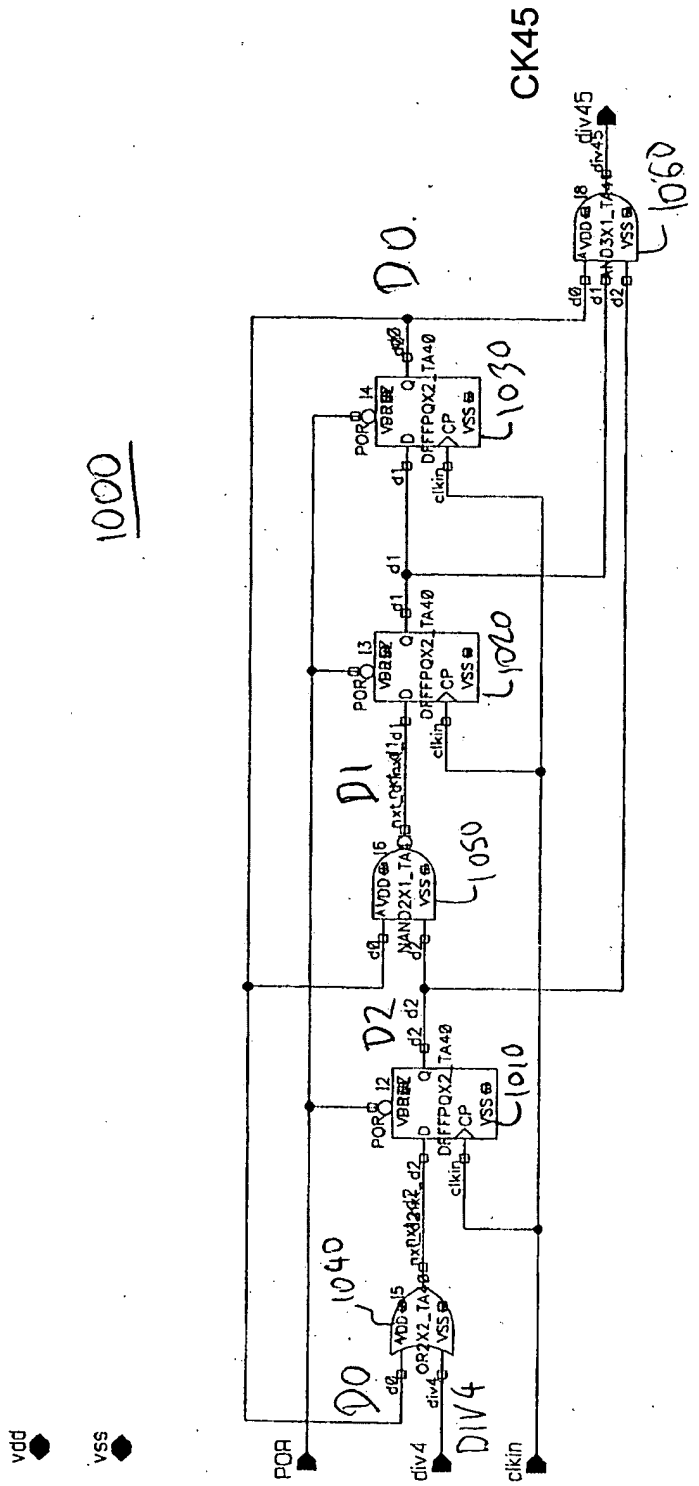

CK45
div45
1000
1060
1030
1020
1050
1010
1040
D0
D1
D2
D0
DIV4
vdd
vss
POR
div4
clkin

FIGURE 10

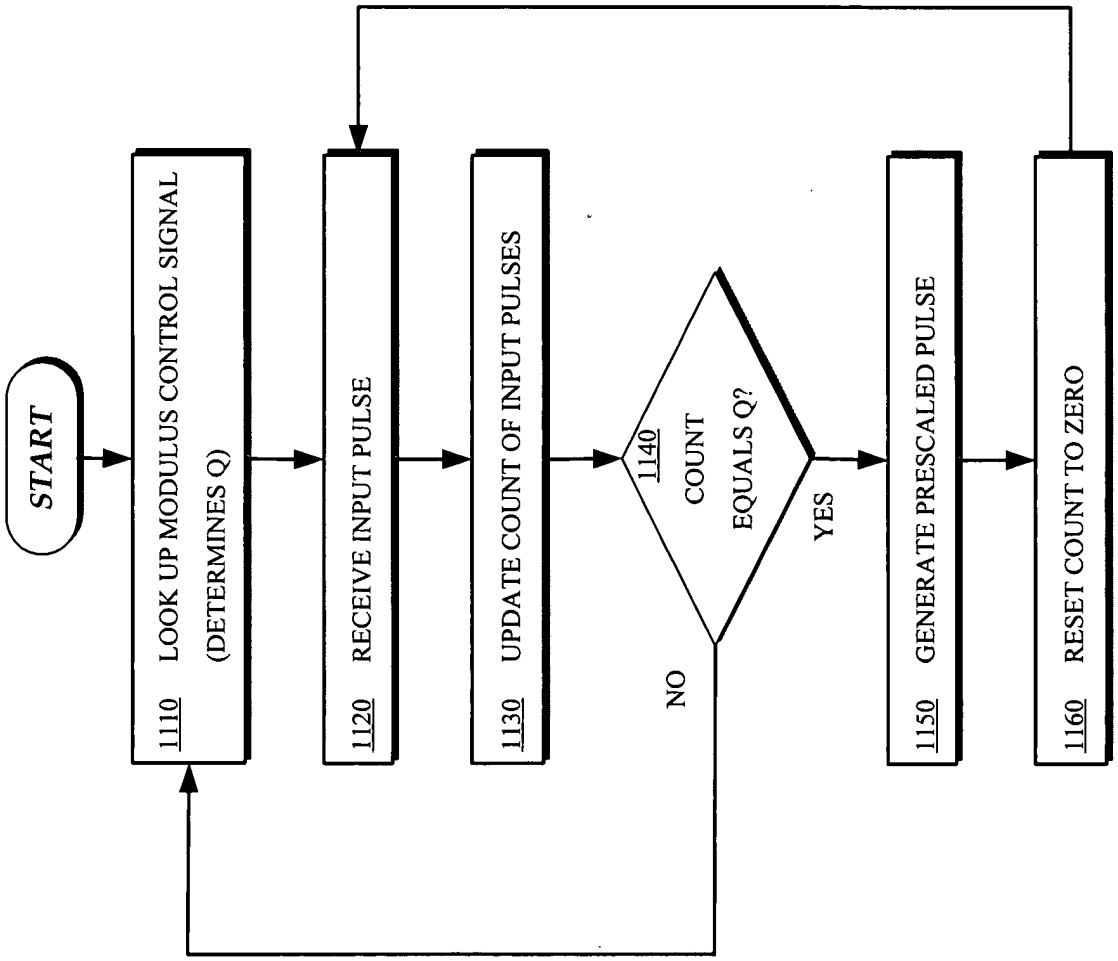

START
1110 LOOK UP MODULUS CONTROL SIGNAL (DETERMINES Q)
1120 RECEIVE INPUT PULSE
1130 UPDATE COUNT OF INPUT PULSES
1140 COUNT EQUALS Q?
NO
YES
1150 GENERATE PRESCALED PULSE
1160 RESET COUNT TO ZERO
1100

FIGURE 11